AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A charge pump circuit comprising:

a first plurality of serially connected transistors of a first conductivity type;

a second plurality of serially connected transistors of a second conductivity type;

said first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors;

the interconnection of said first and second plurality of transistors providing an output~~, said output being adapted to be coupled to a load device~~;

a gate of one of said first plurality of transistors being adapted to receive a $\overline{\text{DOWN}}$ pulse signal, a gate of another one of said first plurality of transistors being adapted to receive a DC bias signal, a gate of one of said second plurality of transistors being adapted to receive an UP pulse signal, and a gate of another one of said second plurality of transistors being adapted to receive another DC bias signal;

a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a DOWN pulse signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive an $\overline{\text{UP}}$ pulse signal; and

a first non-parasitic, non-MOS transistor-based capacitor connected to said first node for applying said DOWN pulse signal to said first node and a second non-parasitic, non-MOS transistor-based capacitor connected to said second node for applying said $\overline{\text{UP}}$ pulse signal to said second node.

2. (Original) A charge pump circuit as in claim 1 wherein said first plurality of transistors are p-channel transistors and said second plurality of transistors are n-channel transistors.

3. (Canceled)

4. (Original) A charge pump circuit as in claim 1 wherein said first plurality of transistors is a pair of transistors and said second plurality of transistors is a pair of transistors.

5-7. (Canceled)

8. (Currently Amended) A charge pump circuit comprising:

a first plurality of serially connected transistors of a first conductivity type;

a second plurality of serially connected transistors of a second conductivity type;

said first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors;

the interconnection of said first and second plurality of transistors providing an output, said output being adapted to be coupled to a load device;

a gate of one of said first plurality of transistors being adapted to receive a first switching signal, a gate of another one of said first plurality of transistors being adapted to receive a DC bias signal, a gate of one of said second plurality of transistors being adapted to receive a second switching signal, and a gate of the other of said second plurality of transistors being adapted to receive another DC bias signal;

a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a complementary first switching signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive a complementary second switching signal; and

a first non-parasitic, non-MOS transistor-based capacitor for applying said complementary first switching signal to said first node and a second non-parasitic, non-MOS transistor-based capacitor for applying said complementary second switching signal to said second node.

9-22. (Canceled)

23. (Currently Amended) A method of operating a charge pump comprising:

switching a first switching transistor in response to a first applied switching signal to affect an output at an output terminal, said output terminal being adapted to be coupled to a load device;

switching a second switching transistor in response to a second applied switching signal to affect an output at said output terminal;

biasing the switching characteristics of said first and second switching transistors with bias transistors respectively serially connected to said first and second switching transistors, said output terminal being connected between said bias transistors;

applying a complementary signal of said first applied switching signal through a first non-parasitic, non-MOS transistor-based capacitor to a connection between said first switching transistor and an associated bias transistor; and

applying a complementary signal of said second applied switching signal through a second non-parasitic, non-MOS transistor-based capacitor to a connection between said second switching transistor and an associated bias transistor.

24. (Previously Presented) A method as in claim 23 wherein said acts of applying comprise capacitive coupling.

25. (Previously Presented) A charge pump circuit as defined in claim 1 wherein said load device comprises a filter of a phase locked loop.

26. (Previously Presented) A charge pump circuit as defined in claim 1 wherein said load device comprises an input of a voltage controlled oscillator.

27. (Previously Presented) A charge pump circuit as defined in claim 1 wherein said first node is adapted to receive said Down pulse signal directly from a phase frequency detector.

28. (Previously Presented) A charge pump circuit as defined in claim 8 wherein said first switching signal is received directly from a phase frequency detector.

29. (Previously Presented) A method of operating a charge pump as defined in claim 23 wherein said first applied switching signal is received directly from a phase frequency detector.